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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/054,393	01/22/2002	David Arnold Luick	ROC920010208US1	8439

7590 01/13/2005

EXAMINER
DO, CHAT C

ART UNIT	PAPER NUMBER
2124	

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DATE MAILED: 01/13/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/054,393	LUICK ET AL.	
	Examiner	Art Unit	
	Chat C. Do	2124	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 January 2002*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *22 January 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Specification

1. Applicant is reminded of the proper language and format for an abstract of the disclosure.

The abstract should be in narrative form and generally limited to a single paragraph on a separate sheet within the range of 50 to 150 words. It is important that the abstract not exceed 150 words in length since the space provided for the abstract on the computer tape used by the printer is limited. The form and legal phraseology often used in patent claims, such as "means" and "said," should be avoided. The abstract should describe the disclosure sufficiently to assist readers in deciding whether there is a need for consulting the full patent text for details.

The language should be clear and concise and should not repeat information given in the title. It should avoid using phrases which can be implied, such as, "The disclosure concerns," "The disclosure defined by this invention," "The disclosure describes," etc.

2. The abstract of the disclosure is objected to because the abstract is written less than 50 words in length. Correction is required. See MPEP § 608.01(b).

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-26 are rejected under 35 U.S.C. 102(b) as being anticipated by McMahan et al. (U.S. 5,337,269).

Re claim 1, McMahan et al. disclose in Figure 1 an Arithmetic and Logic Unit (Figure 1), comprising: at least first and second sub-ALUs (e.g. second ALUs are 12a-12g and first ALUs are 14a-14e), each of the first and second sub-ALUs including a

plurality of slices (e.g. 12a as a slice and 14 a as another slice) wherein the slices of the first and second sub-ALUs are interleaved (e.g. 12a, 14a, 12b, 14b...).

Re claim 2, McMahan et al. further disclose in Figure 1 the slices of the first and second sub-ALus are bitslices (e.g. a[0:1] and b[0:1] input into 12a; C0 and P1 input into 14a).

Re claim 3, McMahan et al. further disclose in Figure 1 each of the bitslices of the first sub-ALU includes a gate configured to perform a logical operation (e.g. NAND logical gate as seen in 14a).

Re claim 4, McMahan et al. further disclose in Figure 1 the gate is configured to receive two input bits and generate one output bit (e.g. 14a in Figure 1).

Re claim 5, McMahan et al. further disclose in Figure 1 the logical operation is logical AND operation (e.g. 14a in Figure 1).

Re claim 6, McMahan et al. further disclose in Figure 1 the bitslices of the first sub-ALU are connected in series (Figure 1 wherein one is connected after another through XOR gate).

Re claim 7, McMahan et al. further disclose in Figure 1 the bitslices of the second sub-ALu are connected in series (Figure 1 wherein one is connected after another through XOR gate).

Re claim 8, McMahan et al. further disclose in Figure 1 each of the bitslices of the first sub-ALU includes an adder (e.g. 12a) configured to add at least two bits to generate a carry bit (e.g. C0 in 10) to a next consecutive bitslice of the first sub-ALU.

Re claim 9, McMahan et al. further disclose in Figure 1 each pair (e.g. 12b, 14a, and 16a) of adjacent bitslices of the ALU comprises a first bitslice of the first sub-ALU (e.g. 12b) and a second bitslice of the second sub-ALU (e.g. 14a and 16a); and wherein: the first bitslice has a first input and a first output (e.g. 12b has Co and C1), a second bitslice has a second input and a second output (e.g. Co and C1); and the first output is connected to the second input (e.g. SC1 into 12c), and the second output is connected to the first input (e.g. C1 of 12b into 16a).

Re claim 10, McMahan et al. further disclose in Figure 1 the slices of the first and second sub-ALus are function slices (e.g. as adder).

Re claim 11, McMahan et al. further disclose in Figure 1 the function slices of the first sub-ALU are connected in series and the function slices of the second sub-ALU are connected in series (e.g. Figure 1).

Re claim 12, McMahan et al. further disclose in Figure 1 a method for implementing at least first and second sub-ALus to form an ALU (e.g. first ALUs as {12a-12g & 16a-16g} and second ALU as 14a-14g), each of the first and second sub-ALus including a plurality of slices, the method comprising: interleaving the slices of the first and second sub-Alus (Figure 1 12a, 14a, 12b, 16a, 14b, 12c...).

Re claim 13, it has same limitations cited in claim 2. Thus, claim 13 is also rejected under the same rationale as cited in the rejection of rejected claim 2.

Re claim 14, it has same limitations cited in claim 6. Thus, claim 14 is also rejected under the same rationale as cited in the rejection of rejected claim 6.

Re claim 15, it has same limitations cited in claim 7. Thus, claim 15 is also rejected under the same rationale as cited in the rejection of rejected claim 7.

Re claim 16, it has same limitations cited in claim 9. Thus, claim 16 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 17, it has same limitations cited in claim 10. Thus, claim 17 is also rejected under the same rationale as cited in the rejection of rejected claim 10.

Re claim 18, it has same limitations cited in claim 11. Thus, claim 18 is also rejected under the same rationale as cited in the rejection of rejected claim 11.

Re claim 19, McMahan et al. further disclose in Figure 1 a method for implementing at least first and second ALUS (e.g. first ALUs as {12a-12g & 16a-16g} and second ALU as 14a-14g), the first ALU having a first input side and a first output side (e.g. 12b), the second ALU having a second input side and a second output side (e.g. 14a), the method comprising: arranging the first and second ALUS using one of first and second arrangements (e.g. parallel arrangement), wherein the first arrangement comprises arranging the first output side closer to the second output side than to the second input side (e.g. two inputs into 16a), the second arrangement comprises arranging the first input side closer to the second input side than to the second output side (e.g. Co).

Re claim 20, McMahan et al. further disclose in Figure 1 arranging the first and second ALUS comprises using the first arrangement (e.g. Co).

Re claim 21, it has same limitations cited in claim 9. Thus, claim 21 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 22, McMahan et al. further disclose in Figure 1 each of the first and second ALUS has at Least first and second sub-Alus (e.g. {12b and 14a to 12c and 14b} and the rest are second sub-ALUs), each of the first and second sub-ALus including a plurality of slices wherein the slices of the first and second sub-ALUS are interleaved (e.g. 12a, 14a, 12b, 16a, 14b...).

Re claim 23, it is a digital circuit claim of claim 19. Thus, claim 23 is also rejected under the same rationale as cited in the rejection of rejected claim 19.

Re claim 24, it has same limitations cited in claim 9. Thus, claim 24 is also rejected under the same rationale as cited in the rejection of rejected claim 9.

Re claim 25, it is a digital circuit claim of claim 22. Thus, claim 25 is also rejected under the same rationale as cited in the rejection of rejected claim 22.

Re claim 26, McMahan et al. further disclose in Figure 1 the slices of the first and second sub-ALus comprises one of bitslices and function slices (e.g. as adder).

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. U.S. Patent No. 5,974,437 to Johannsen discloses a fast array multiplier.

b. U.S. Patent No. 5,081,607 to Bates et al. disclose an arithmetic logic unit.

c. U.S. Patent No. 5,390,135 to Lee et al. disclose a parallel shift and add circuit and method.

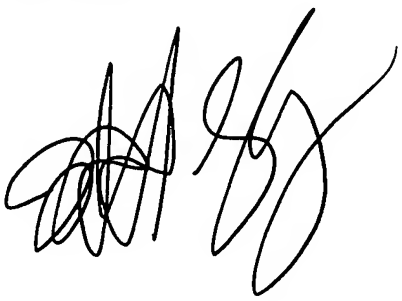
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Chat C. Do whose telephone number is (571) 272-3721. The examiner can normally be reached on M => F from 7:00 AM to 5:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Chaki Kakali can be reached on (571) 272-3719. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Chat C. Do
Examiner
Art Unit 2124

January 7, 2005



TODD INGBERG
PRIMARY EXAMINER